UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,957	07/27/2001	Manish Sinha	218.1029	9342

7590 06/03/2004

Davidson, Davidson & Kappel, LLC
485 Seventh Avenue, 14th Floor
New York, NY 10018

EXAMINER
MASKULINSKI, MICHAEL C

ART UNIT	PAPER NUMBER
2113	6

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,957	SINHA ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/ 16 April 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 9-11, 13-23, and 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Nelvin et al., U.S. Patent 6,708,283 B1.

Referring to claims 1 and 21:

a. In column 2, lines 20-21, Nelvin et al. disclose a virtual path that includes at least a virtual peripheral bus controller and a virtual video controller (identifying a virtual device associated with a first slot of a plurality of slots)

b. In column 4, lines 44-54, Nelvin et al. disclose that there are redundant peripheral bus controllers and video controllers on PCI busses 0 and 1 (identifying a backup I/O component in a second slot of the plurality of slots)

c. In column 5, lines 39-53, Nelvin et al. disclose that if one of the selected controllers should fail, the system performs fail-over operation to change its controller selections and in response changes the setting in the configuration registers on each of the CPU boards to give the previously unselected controllers

access to the I/O address space in the memory (disassociating the virtual device with the first slot and associating the virtual device with the second slot).

Referring to claims 2 and 22, in column 5, lines 39-53, Nelvin et al. disclose detecting that a controller has failed (prior to the identifying a virtual device step, the method includes the step of detecting a failure of an I/O component in the first slot).

Referring to claims 3 and 23, in column 5, lines 26-33, Nelvin et al. disclose that the system uses a peripheral bus configuration register on the CPU board, or at least one predetermined bit location in the register, to establish which controllers may claim the I/O address space in the memory (wherein the identifying a virtual device step comprises accessing a virtual device data structure to identify the virtual device associated with the first slot, the virtual device data structure maintaining an association between a plurality of virtual devices and at least a sub-set of the plurality of slots).

Referring to claims 4, 16, and 20, in column 6, lines 40-47, Nelvin et al. disclose that diagnostic routines performed by a system hardware manager and/or error detection logic, which are resident in whole or in part on a mother board into which the I/O boards plug, inform a system hot plug controller and the I/O system manager that a device resident on a particular I/O board, such as the peripheral bus controller has failed (wherein the step of detecting a failure is performed by a Hot Swap Management System).

Referring to claim 5, in column 8, lines 52-58, Nelvin et al. disclose that when the front panel is removed, the I/O system manager notices the change and notifies the plug and play manager. The plug and play manager requests a PCI bus enumeration,

and the HAL functions then tell the plug and play manager that certain peripheral devices are no longer connected, and the plug and play manager determines that the user should be notified (wherein the failure is caused by removal of the I/O component from the first slot).

Referring to claims 9 and 25, in column 5, lines 26-33, Nelvin et al. disclose that the system uses a peripheral bus configuration register on the CPU board, or at least one predetermined bit location in the register, to establish which controllers may claim the I/O address space in the memory. The register bit is thus set to the appropriate value to select, as appropriate, the controllers connected to the PCI bus 0 at the CPUs or the controllers connected to the PCI bus 1 at the CPUs (generating a system configuration data structure, the system configuration data structure including an entry for each slot of the plurality of slots, each entry including information indicative of an expected I/O device for the corresponding slot and an I/O parameter for the expected I/O device; and generating the virtual device data structure as a function of the system configuration data structure).

Referring to claims 10 and 27, in column 5, lines 44-49, Nelvin et al. disclose that the I/O system manager on the south side of the other PCI-to-PCI bridges is notified of the failure, and responds by changing the setting in the configuration registers on each of the CPU boards, to give the previously unselected controllers access to the I/O address space in the memory. The I/O system manager also changes the control setting of the switches, such that the switches use peripheral busses associated with

the newly selected set of controllers (wherein the I/O parameter includes a plurality of I/O parameters).

Referring to claims 11 and 28, in column 5, lines 44-49, Nelvin et al. disclose that the I/O system manager on the south side of the other PCI-to-PCI bridges is notified of the failure, and responds by changing the setting in the configuration registers on each of the CPU boards, to give the previously unselected controllers access to the I/O address space in the memory. The I/O system manager also changes the control setting of the switches, such that the switches use peripheral busses associated with the newly selected set of controllers (wherein the expected I/O device includes a plurality of expected I/O devices, and wherein the I/O parameter includes one or more I/O parameters for each of the plurality of expected I/O devices).

Referring to claims 13 and 26, in column 5, lines 44-49, Nelvin et al. disclose that the I/O system manager on the south side of the other PCI-to-PCI bridges is notified of the failure, and responds by changing the setting in the configuration registers on each of the CPU boards, to give the previously unselected controllers access to the I/O address space in the memory. The I/O system manager also changes the control setting of the switches, such that the switches use peripheral busses associated with the newly selected set of controllers (disassociating the virtual device from a first driver, the first driver being a driver for an I/O component in the first slot; associating the virtual device with a virtual driver; identifying a second driver, the second driver being a driver for the backup I/O component in the second slot; disassociating the virtual device from the virtual driver; and associating the second driver with the virtual device).

Referring to claims 14 and 18:

a. In column 5, lines 26-33, Nelvin et al. disclose that the system uses a peripheral bus configuration register on the CPU board, or at least one predetermined bit location in the register, to establish which controllers may claim the I/O address space in the memory (a virtual device data structure, the virtual device data structure maintaining an association between a plurality of virtual devices and a plurality of slots in a chassis).

b. In column 5, lines 39-53, Nelvin et al. disclose detecting that a controller has failed (a failure detection component, the failure detection component being capable of detecting a failure of an I/O component in one of the plurality of slots).

c. In column 5, lines 44-49, Nelvin et al. disclose that the I/O system manager on the south side of the other PCI-to-PCI bridges is notified of the failure, and responds by changing the setting in the configuration registers on each of the CPU boards, to give the previously unselected controllers access to the I/O address space in the memory. The I/O system manager also changes the control setting of the switches, such that the switches use peripheral busses associated with the newly selected set of controllers (a disconnect component, the disconnect component being capable of disassociating the I/O component from a corresponding one of the virtual devices associated with the one of the plurality of slots holding the I/O component, and identifying a backup I/O component in another one of the plurality of slots based upon the virtual device data structure; a connect component, the connect component being capable of

associating the corresponding one of the virtual devices with the backup I/O component).

Referring to claims 15 and 19, in column 5, lines 39-53, Nelvin et al. disclose an I/O system manager for disconnecting and connecting components (the disconnect component and the connect component are implemented in software).

Referring to claim 17:

a. In column 5, lines 17-23, Nelvin et al. disclose having a plurality of peripheral bus and video controllers. Further, in column 5, lines 39-41, Nelvin et al. disclose providing fail-over operations for the controllers (a plurality of I/O components secured within respective slots in a chassis, at least two of the plurality of I/O components forming a peripheral failover pair).

b. In column 5, lines 44-49, Nelvin et al. disclose that the I/O system manager on the south side of the other PCI-to-PCI bridges is notified of the failure, and responds by changing the setting in the configuration registers on each of the CPU boards, to give the previously unselected controllers access to the I/O address space in the memory. The I/O system manager also changes the control setting of the switches, such that the switches use peripheral busses associated with the newly selected set of controllers (a peripheral failover system, the peripheral failover system detecting a failure of one I/O component in the peripheral failover pair and disassociating a virtual device from the failed I/O component and associating the virtual device with the other I/O component in the peripheral failover pair).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 7, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelvin et al., U.S. Patent 6,708,283 B1, and further in view of Lipe et al., U.S. Patent 5,748,980.

Referring to claims 6 and 24, in column 7, lines 51-64, Nelvin et al. disclose that when a new device is plugged into the slot, to replace a failed device, the hot plug controller applies power to the slot and the device boots, to establish its clock and logic levels. However, Nelvin et al. don't explicitly disclose disassociating the virtual device from a first driver, the first driver being a driver for an I/O component in the first slot; identifying a second driver, the second driver being a driver for the backup I/O component in the second slot; and associating the second driver with the virtual device. In column 383, lines 20-24, Lipe et al. disclose that the device configuration system detects the presence of the devices on each of the system busses, allocates resources to each of the detected devices, and directs the automated loading of device drivers for the detected devices. It would have been obvious to one of ordinary skill at the time of the invention to include the device configuration system of Lipe et al. into the system of Nelvin et al. A person of ordinary skill in the art would have been motivated to make the

modification because automation of the configuration process supplies the advantage of removing the user from these configuration tasks (see Lipe et al.: column 383, lines 30-32.

Referring to claim 7, in column 26, lines 9-21, Nelvin et al. disclose that a device driver program can be downloaded from a floppy disk to a mass storage memory device (downloading the second driver from a host system).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Nelvin et al., U.S. Patent 6,708,283 B1 and Lipe et al., U.S. Patent 5,748,980, and further in view of Kitagawa, US 2002/0194583 A1.

Referring to claim 8, in column 383, lines 20-24, Lipe et al. disclose that the device configuration system detects the presence of the devices on each of the system busses, allocates resources to each of the detected devices, and directs the automated loading of device drivers for the detected devices. However, neither Nelvin et al. nor Lipe et al. disclose downloading the second driver from the Internet. In paragraph 0055, Kitagawa disclose downloading a device driver from the Internet. It would have been obvious to one of ordinary skill at the time of the invention to include the ability of downloading a device driver from the Internet of Kitagawa into the combined system of Nelvin et al. and Lipe et al. A person of ordinary skill in the art would have been motivated to make the modification because a device driver is not always available from the system or an updated driver is necessary (see Kitagawa: paragraph 0054). The system of Kitagawa provides the necessary device driver.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nelvin et al., U.S. Patent 6,708,283 B1, and further in view of Nguyen et al., U.S. Patent 6,055,600.

Referring to claim 12, in column 5, lines 39-53, Nelvin et al. disclose that the I/O component is a PCI controller. However, Nelvin et al. don't explicitly disclose that the I/O component is one of an ethernet card, a serial port, a parallel port, and an SCSI device. In Figure 1, Nguyen et al. disclose a PCI Bridge controller connected to a parallel port, a serial port, a SCSI I/O processor, and an Ethernet controller. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel port, a serial port, a SCSI I/O processor, and an Ethernet controller of Nguyen et al. into the system of Nelvin et al. A person of ordinary skill in the art would have been motivated to make the modification because all of these components are compatible with a PCI I/O controller and are common devices in a computer system.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,735,715 B1 Graham

U.S. Patent 6,742,136 B2 Christensen et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100